Technology Advances for Pilot line of Enhanced Semiconductors for 3nm
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Senior Project Manager

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Amsterdam

“This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 783247. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, United Kingdom, Israel, Switzerland.”
The world has been **improving computer power** for 120 years. 18 orders of magnitude increase of calculation speed per dollar, and still continuing.

Source: Ray Kurzweil, Steve Jurvetson
TAPES3 goal: To enable Semiconductor Industry to progress to the 3nm node
By reducing minimum feature size.....
TAPES3 goal: To enable Semiconductor Industry to progress to the 3nm node

...and by improving technology for chip manufacture

From 2D To 3D

Gate All Around a larger surface on the same size

Super Vias and Buried Power Rail to cram more transistors in the same area

“Making things smaller to make greater things”
TAPES3 - 4 pillars

**Lithography**
- Numerical Aperture 0.33 → 0.55
- Optics & Image performance
- Productivity

**Mask Infrastructure**
- Absorber materials & processing
- Mask tuning, repair & Inspection
- Mask storage effects

**Metrology**
Measurement solutions for:
- High Aspect Ratio and gate all around stacked features
- Smaller dimension & alignment

**Process Technology**
- Patterning
- Device & Interconnect options
- Yield prediction, wafer handling
- Scaling boosters
TAPES3: Pillars & project partners
A unique ECO system of semiconductor expertise united around imec’s pilot-line

Lithography
- ASML

Metrology
- Applied Materials

Mask Infrastructure
- imec

Process Exploration
- imec

Large Industry
- ZEISS
- VDL
- Applied Materials
- KLA
- Zeiss
- SUSS MicroTec
- siltronic
- Siemens
- ASML
- DEMCON

SME
- optiXfab
- ibs
- REPIF

RTO & University
- Fraunhofer
- imec

26 Partners in 7 countries, Belgium, Germany, France, United Kingdom, Israel, Switzerland and The Netherlands
Impact: Worldwide…

TAPES3 supports the chip industry to continue its worldwide growth from $0.6 trillion to $1.0 trillion in 2030

… closer to home …
Thank you

Please visit our “More Moore” booth

Amsterdam

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Continuing effort in pushing technological boundaries

14 Angstrom CMOS technology
Integration of processes and modules for the 2nm node meeting Power Performance Area and Cost requirements

IC Technology for the 2nm Node

Pilot Integration 3nm Semiconductor Technology
Technology Advances for Pilot line of Enhanced Semiconductors for 3nm

ASML
November 29, 2022