



Technology Advances for Pilot line of Enhanced Semiconductors for 3nm

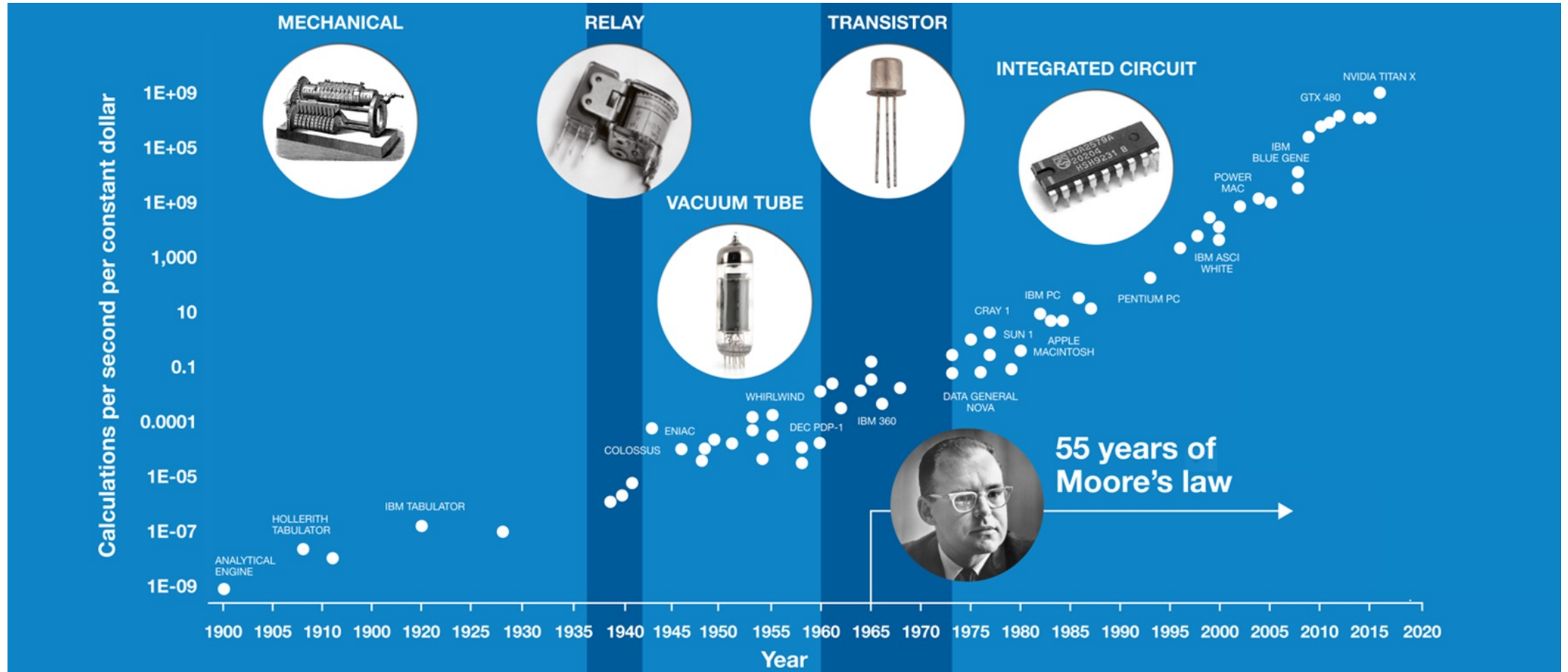
Frans List
Senior Project Manager

EFECS November 25, 2022
Amsterdam



"This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 783247. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, United Kingdom, Israel, Switzerland."

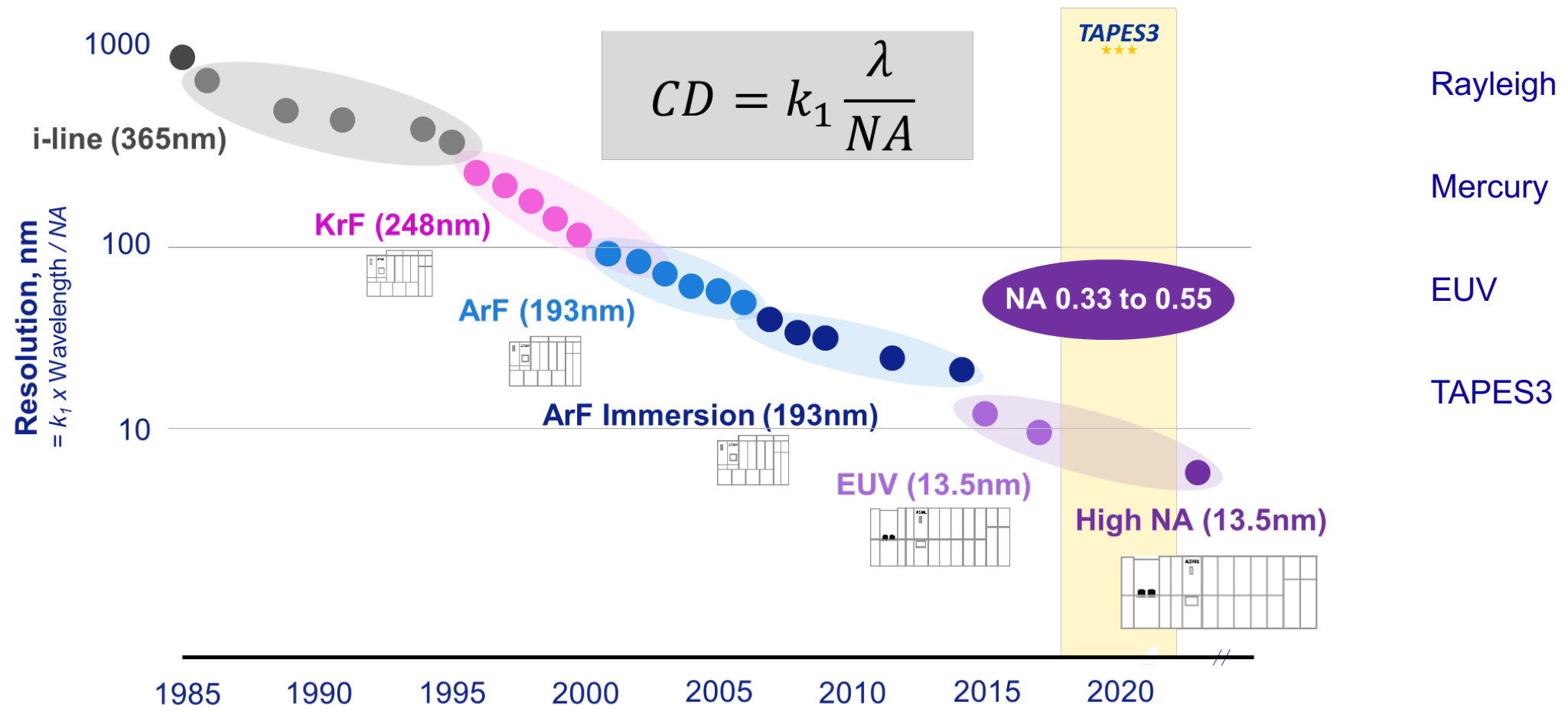
The world has been **improving computer power** for 120 years
18 orders of magnitude increase of calculation speed per dollar, and still continuing



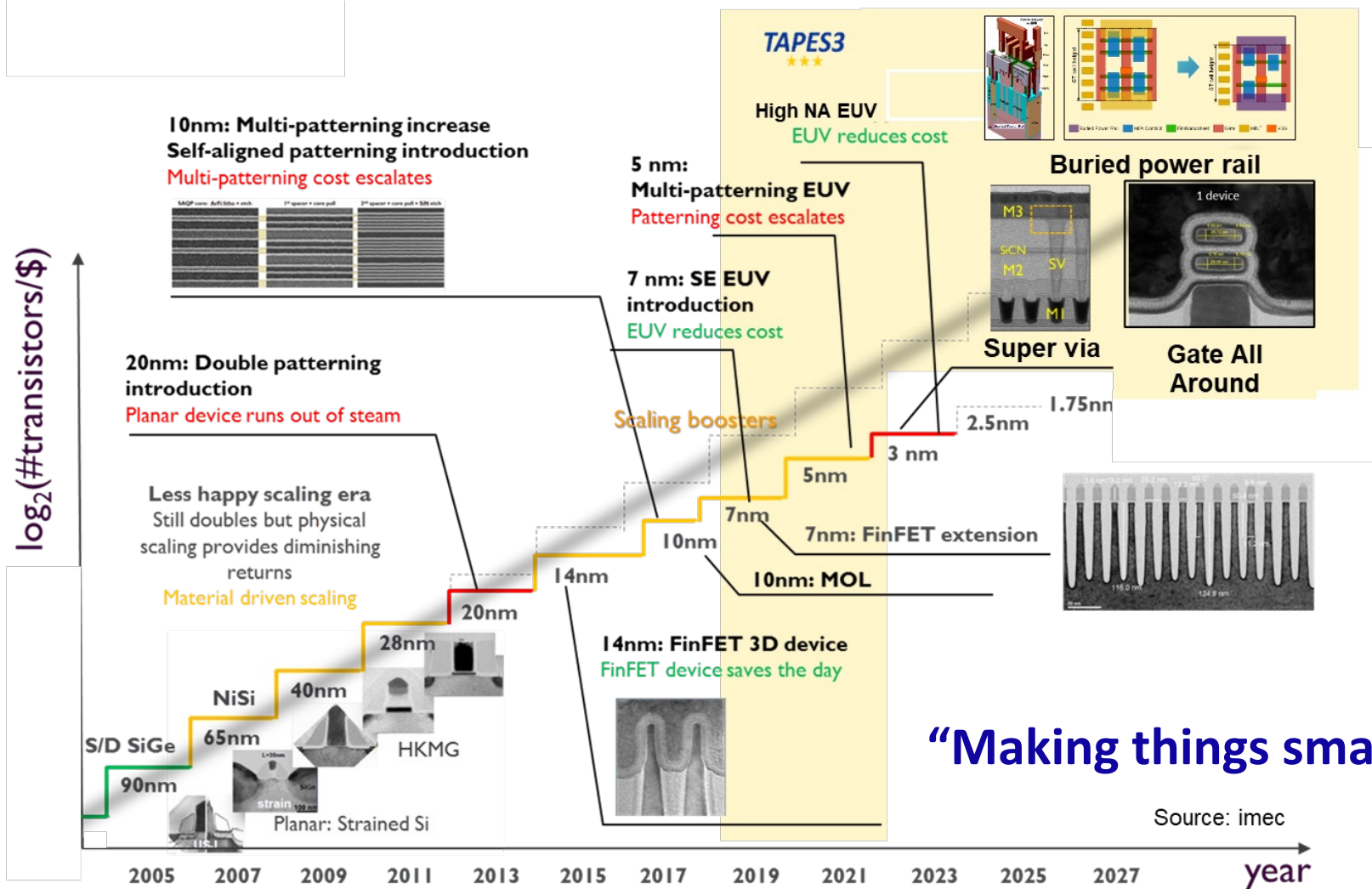
Source: Ray Kurzweil, Steve Jurvetson

TAPES3 goal: To enable Semiconductor Industry to progress to the 3nm node

By reducing minimum feature size.....



TAPES3 goal: To enable Semiconductor Industry to progress to the 3nm nodeand by improving technology for chip manufacture



From 2D To 3D

Gate All Around a larger surface on the same size

Super Vias and Buried Power Rail to cram more transistors in the same area

“Making things smaller to make greater things”

TAPES3 - 4 pillars

DOE prototype meeting specs

- 150nm resolution
- Uniform within Ø404mm

Realization of the High-NA Position Module Qualification Tool

First 0.55NA EUV tool modules integrated

ASML

DEMS chips

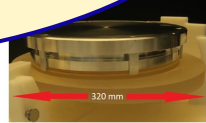
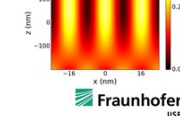
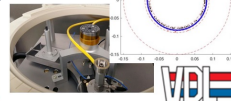
DEMCON

Lithography

- Numerical Aperture 0.33 → 0.55
- Optics & Image performance
- Productivity

First 0.55NA EUV Mech P prototype was finalized

ZEISS



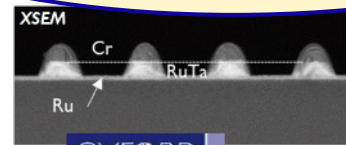
Fraunhofer IWS

RWTH AACHEN UNIVERSITY

ZEISS

Mask Infrastructure

- Absorber materials & processing
- Mask tuning, repair & Inspection
- Mask storage effects

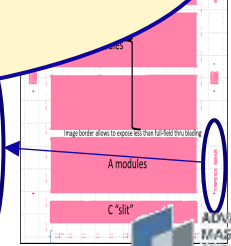


OXFORD INSTRUMENTS
The Business of Science

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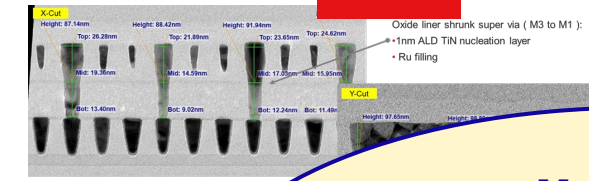


TAPES3 ROADMAP



ADVANCED MASK TECHNOLOGY CENTER

ThermoFisher SCIENTIFIC



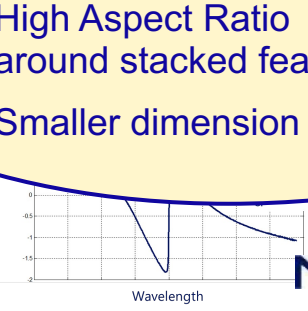
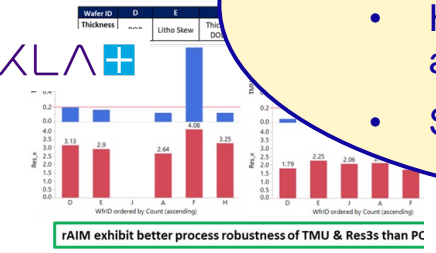
APPLIED MATERIALS

Metrology

Measurement solutions for:

- High Aspect Ratio and gate all around stacked features
- Smaller dimension & alignment

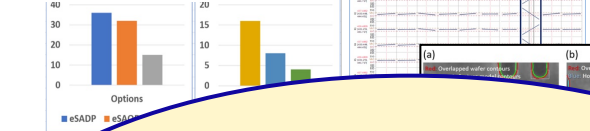
KLA



NOVA PROCESS INSIGHT

imec

COVENTOR

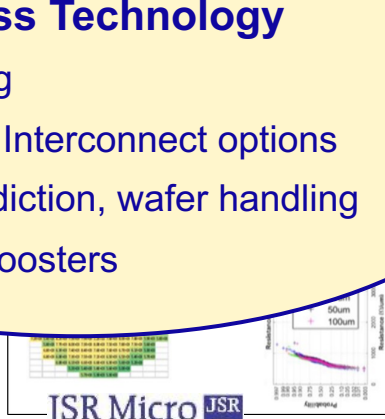
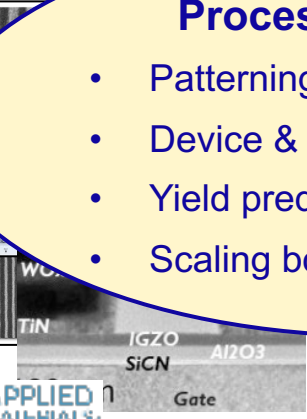
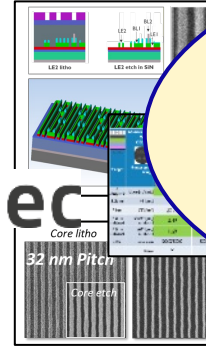


SIEMENS

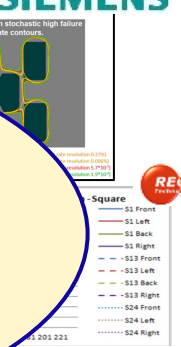
Process Technology

- Patterning
- Device & Interconnect options
- Yield prediction, wafer handling
- Scaling boosters

imec



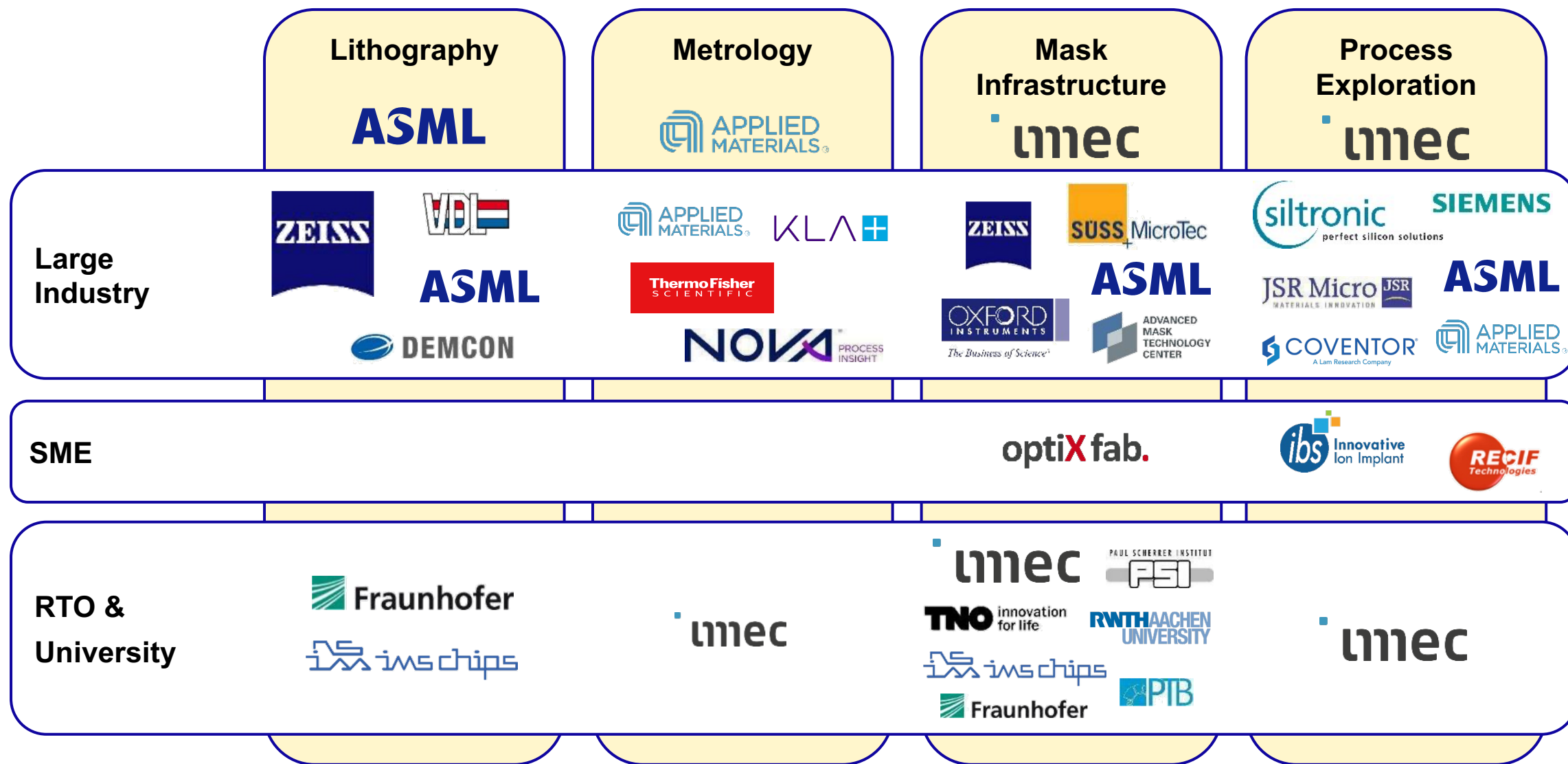
RECIF



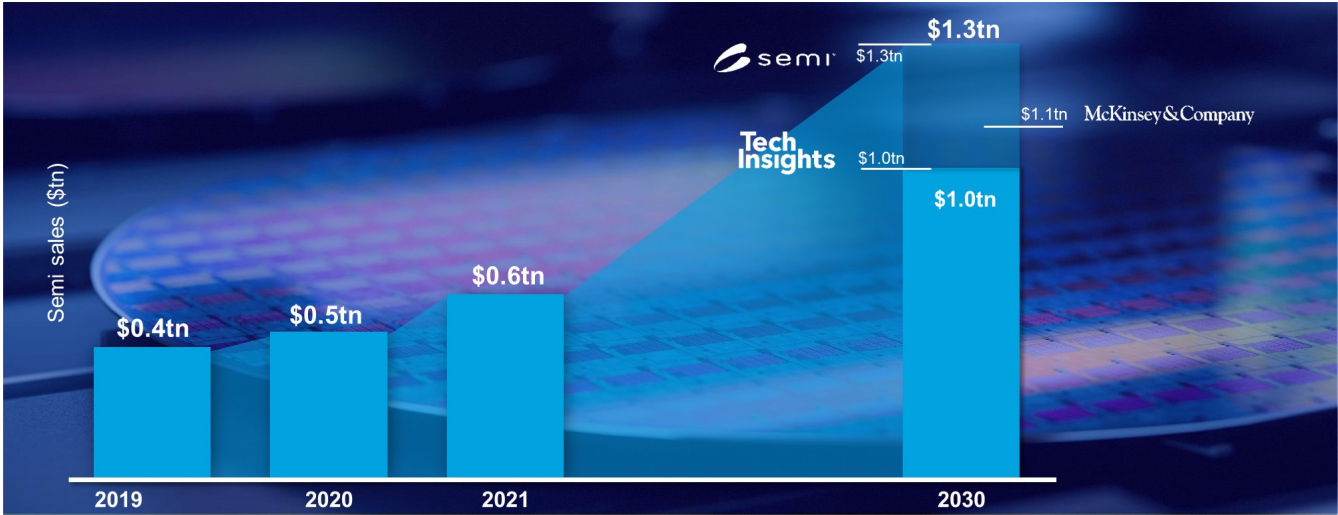
JSR Micro

TAPES3: Pillars & project partners

A unique ECO system of semiconductor expertise united around imec's pilot-line



Impact: Worldwide...



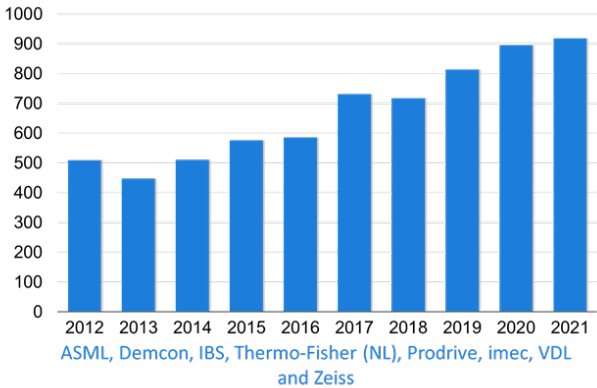
Sources: TechInsights, McKinsey, SEMI.org

TAPES3 supports the chip industry to continue its worldwide growth from \$0.6 trillion to \$1.0 trillion in 2030

... closer to home ...

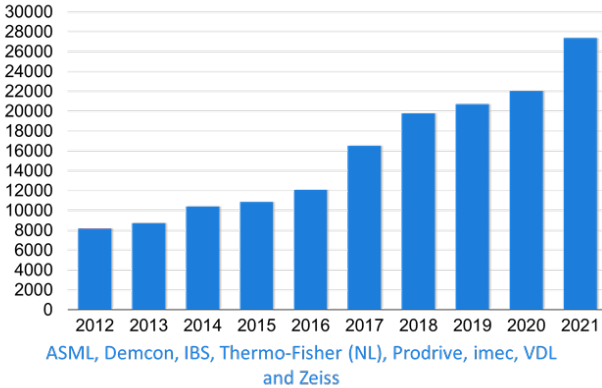
Knowledge creation

- Number of First Patent Filings per year



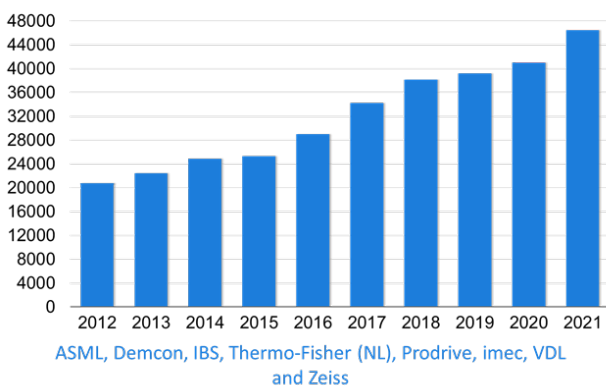
Value creation

- Net sales (M€) in Litho-, Metrology- and Process Equipment per year



Job creation

- # of highly skilled jobs over the years



Thank you



Please visit our “More Moore”
booth



Amsterdam

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Continuing effort in pushing technological boundaries

