APECS – European Chiplet Innovation

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Dec 5, 2024

APECS Pilot Line

Importance of Heterogeneous Integration

Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

- is key for next generation of More-than-Moore capabilities
- meets the needs of European industry with a variety of vertical applications served by mature nodes and specialized technologies such as power, opto/RF, MEMS
- drives performance in many vertical applications such as automotive, medical, industry, aerospace

The APECS Pilot Line will

- build upon FMD's strengths in collaboration and joint innovation with industry partners
- provide access to advanced hetero-integration / advanced packaging technologies for industry (in particular SMEs, small volume)

APECS is co-funded by the Chips Joint Undertaking and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain, through the Chips for Europe Initiative.

APECS
European Chiplet Innovation

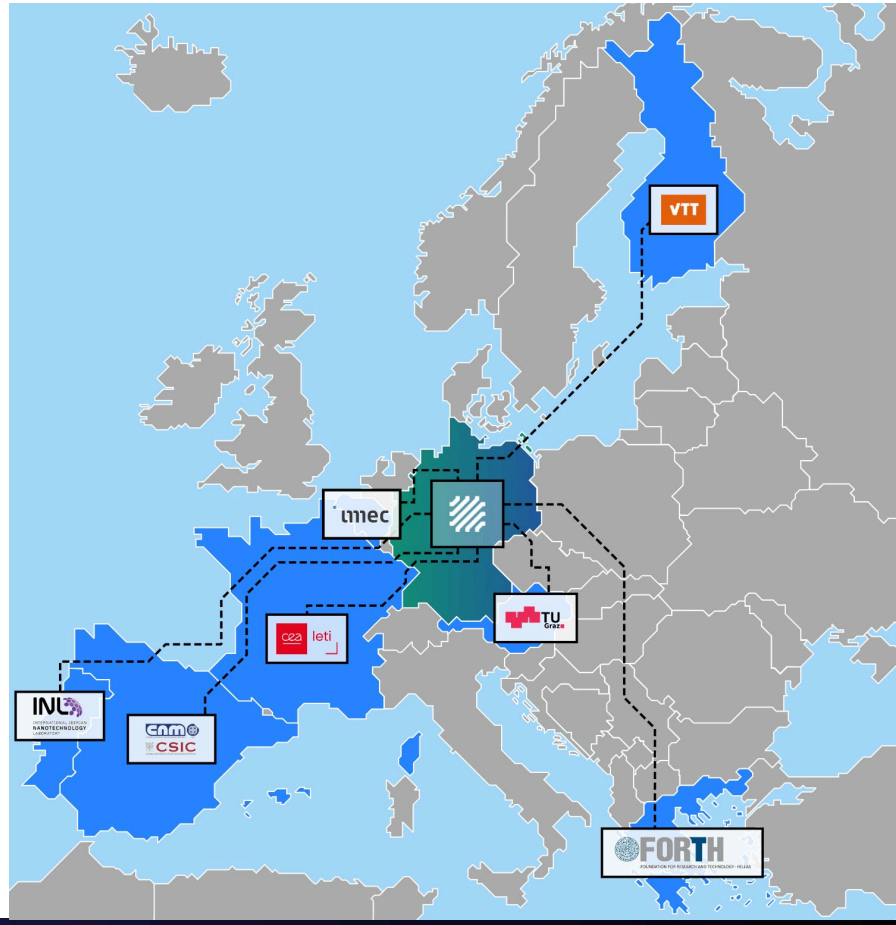
KEY FACTS

- 730 Mio EUR total budget
- Expected start Q4/2024
- Operational end Q2/2029

APECS Pilot Line

Groundbreaking Infrastructure for Heterogeneous Integration

- Bundling the know-how of our partners
- Offering services, capabilities, and training for European companies and research organizations
- Integration and packaging of chiplets and further advanced electronic components into novel electronic systems
- Joining forces with Europe's leading RTOs
- Developing a platform of capabilities that includes:
  - Novel characterization
  - Quality assurance
  - Testing and reliability methodologies
  - System-Technology Co-Optimization (STCO) design framework
- Ensuring quality, reliability, security, green manufacturing, and fast production ramp-up
- Collaboration with manufacturing organizations



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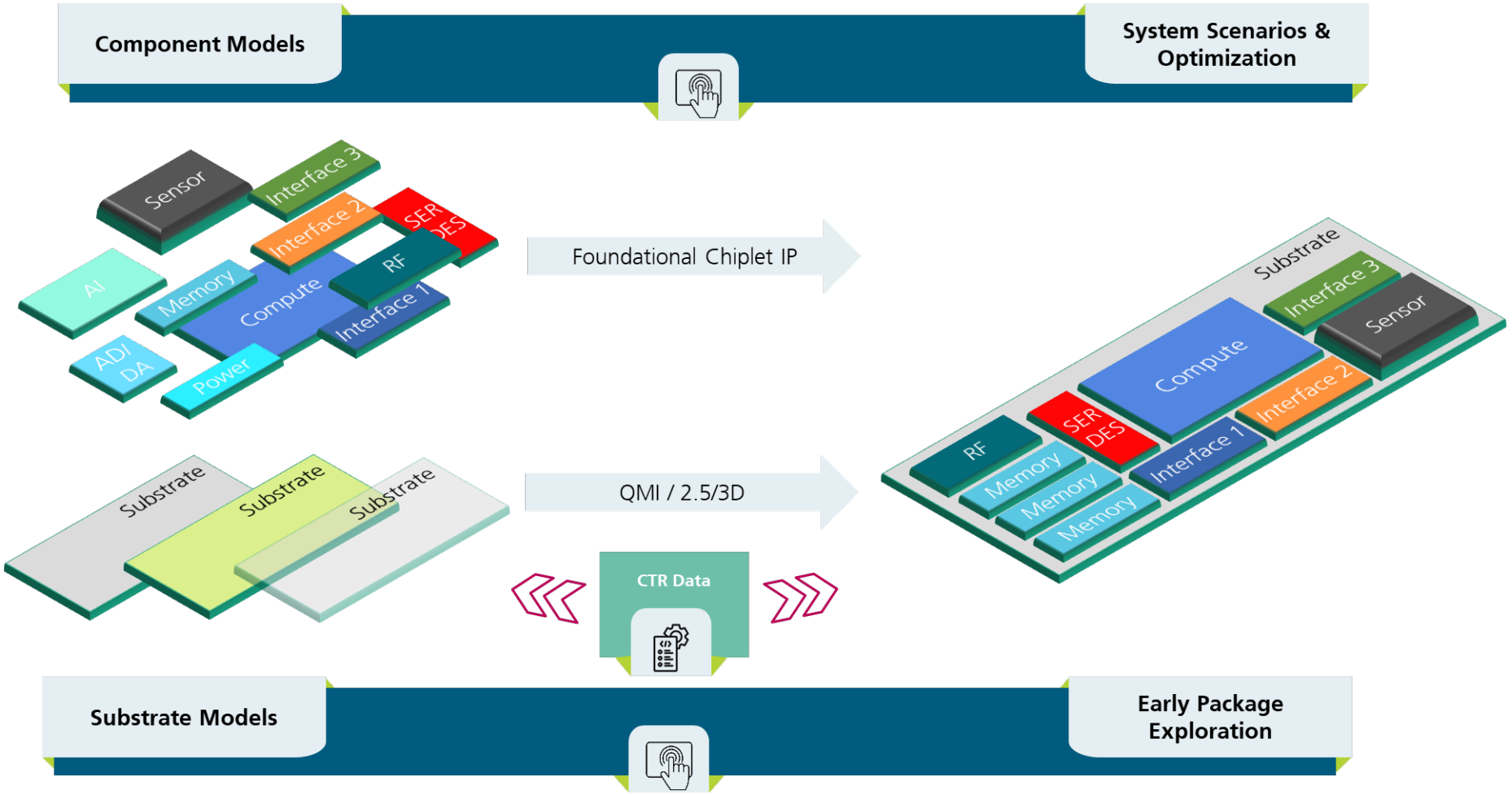

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Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

P/ADK Design Flows
- STCO Design

Interface Processing
- Chiplet Integration
  - Hetero-integration into (quasi-) monolithic integration
  - Chiplet Integration platform (2.5D and 3D)

Analysis & Metrology
- Characterization, Test & Reliability

Users
- SMEs
- Start-ups
- System / Design Houses
- IDMs
- RTOs
- Universities

Application Solution developed under the EU Green Deal

Partners:

Fraunhofer MIKROELEKTRONIK · FBH · VTT · TU Graz · VTT · imec · cea leti · FORTH · CSIC · INL

APECS Pilot Line

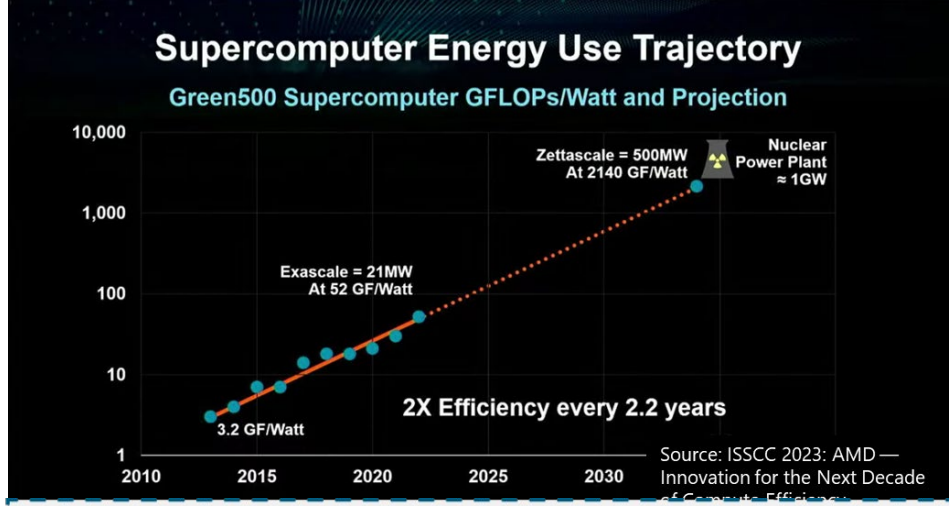
Trends in Technology-Research

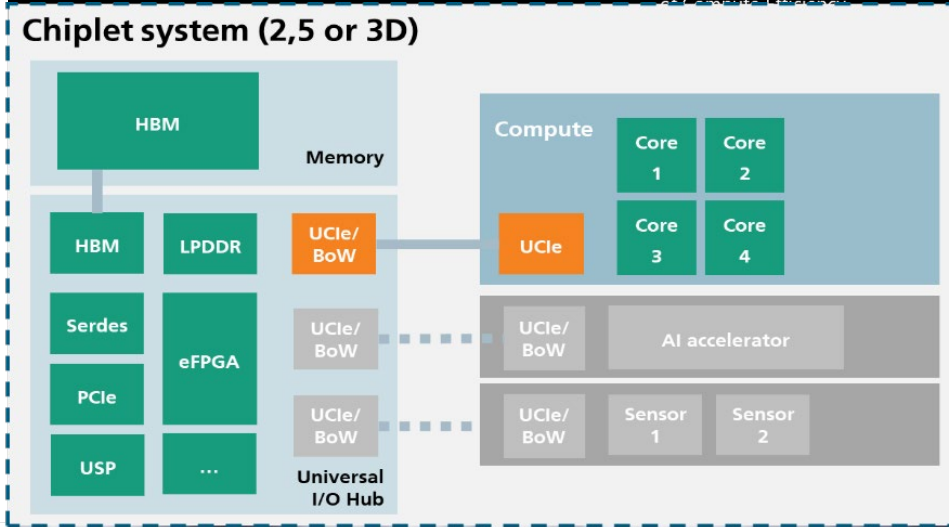
High-performance computing is increasingly energy hungry

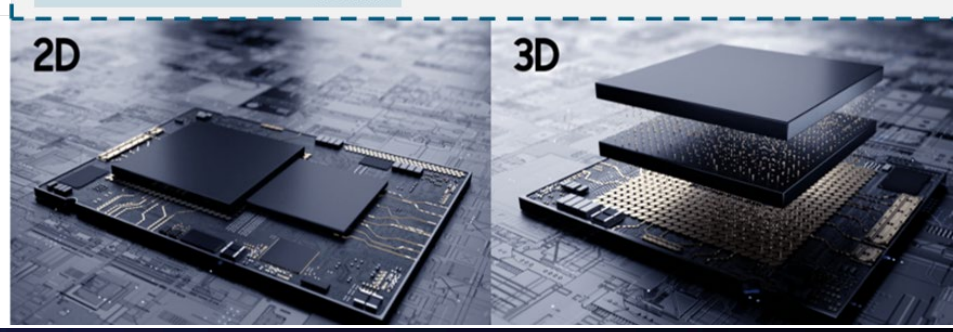
- Main source is higher number of FLOPs/s and massively growing bandwidth demand of high-speed interconnects
- Energy efficiency is driven by System Level Optimization
- New compute architectures (e.g. neuromorphic)
- Combination of Advanced Node & Hetero-Integration for advanced computing

More-than-Moore for Lower Power

- Functional integration in one package
- Driving HPC performance in chiplets







APECS Pilot Line

Main Topics

1

- **End-to-end system/chip design** for Function
- Testability / Yield optimization
- Reliability
- Security

2

- **Technological backend process chains** (CMOS, MEMS, Photonics, Power)
- for component and chiplet integration
- different substrates (organic, glass core, silicon)
- advanced packaging

3

- **Characterization, Test & Reliability** (CTR) for fault location and analysis
- Test concepts for yield optimization

4

- **Support of objectives of the European Green sustainable technologies**
- minimizing energy consumption, reducing environmental impact
- and enhancing resource efficiency

APECS Pilot Line – Expected Outcomes

- **Advanced technologies for customized applications**
  Innovation in advanced packaging and heterogeneous system integration using chiplets, QMI, RF, opto, sensor, and passive components
- **Breakthrough process integration concepts**
  APECS connects theoretical innovation with practical application, enabling next-level integration technologies from system design to testing and security
- **Reduced Time-to-Market**
  APECS streamlines the design of processes for advanced heterogeneous integration from initial design to testing
- **Long-term accessibility**
  A sustainable pilot line providing SMEs and startups with long-term autonomous access to services and infrastructure
- **Smooth knowledge transfer**
  APECS pilot line facilitates reliable knowledge transfer between RTOs to accelerate made-in-Europe innovation
- **Attracting and retaining talent**

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APECS Pilot Line

Open Chiplet and Heterogeneous Integration Platform

User


Chip Foundries


Integrated Device Manufacturer (IDMs)


Materials & Tools Supplier


Semiconductor Customer


Research Community


Start-ups

Value Proposition

- **Design services to create and expand businesses**
  - **Design enablement** for chips, chiplet IPs, and systems to be manufactured in the APECS Pilot Line
  - Provision and operation of **design platforms with corresponding support**
- **Process development, materials and tool validation**
  - Accelerated development of **technology and validated processes**
  - **focus on transferability** into commercial production lines
- **System development**
  - Use of APECS technologies to **create new products and business offerings**
  - Easy access to specialized technologies for products of higher complexity
- **Outsourcing for manufacturing**
  - **Proof of Concept**, Demonstrators with high TRL / low volume production
  - **Prototype runs** and **small volume business**
  - Options to transfer high innovative products with volume forecast
- **Access to research facilities for Academia & European RTOs**
  - Support to expedite transfer of research results into applications
  - Easy access to APECS Platforms via **local Member State Competence Center**

Thanks for Your Attention

Contact

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