



NanolC

Accelerating chip innovation beyond 2 nm

Challenges and objectives

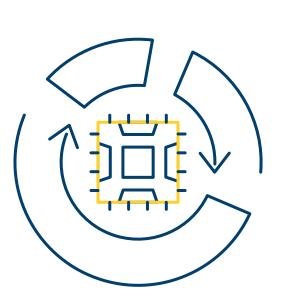


The NanolC project aims to fulfil the European Chips Act's vision for leadership and competitiveness in advanced system-on-chip (SoC) innovation.

Critical markets requiring high integration and efficiency will be strongly impacted by these technologies \rightarrow high-performance computing, energy, AR/VR, automotive, and healthcare.

Technical goals

R&D enablement to prepare the relevant **platforms** in the field of



ADVANCED LOGIC

NanoSheet FET and CFET architectures, enabling HNA EUV pattering capabilities

At die and wafer level

ADVANCED INTERCONNECTS

NanolC

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NOVEL EMBEDDED MEMORIES SOT-MRAM, eDRAM, 3D-DRAM

With the aim to **develop**, optimize and mature baseline flows, enabling the relevant technical capability while strongly increasing repeatability, reducing variability and defectivity \rightarrow towards platforms to enable early access.

Expected impact

-> PDKs for virtual prototyping of new system architectures and prototyping using foundry logic wafers;

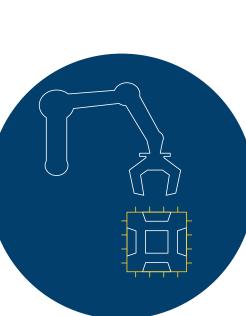
-> Training initiatives and collaborations with universities and research organizations.

European outreach to all actors in the supply chain:



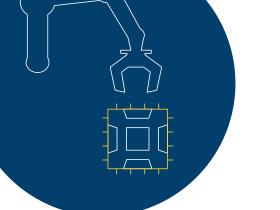
START-UPs, SMEs, UNIVERSITIES AND DESIGN COMPANIES: early access to PDKs for pathfinding and prototyping





EQUIPMENT AND MATERIALS SUPPLIERS: test and refine new tools and processes

Additional information



IDMs, FOUNDRIES: leverage baselines to explore new module and performance enhancement options

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-> European competitiveness across the entire industry value chain: from semiconductor materials and processes, to designs, systems, and applications.





